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Switching arrangement including time-slot buses and several buffers.

Field of the invention

The present invention is related to data nodes in communication networks, in particular to transmitting independent serial data streams through synchronous Time Division Multiplexing (TDM) switches.

Background of the invention

The lower layer of communication networks like the connectivity layer in a core network of a cellular environment could be seen as a layer of distributed resources for managing data flows. Switches and multiplexers are some of the main components for this purpose. In complex communication networks managing data of different formats and varying data rates, it is of great importance that the construction of the components are flexible without being too complex.

Conventionally, the switches comprise a number of serial inputs and outputs. The data stream of one input may be directed in its entirety to a certain output line, or it may consist of a mixture of time division multiplexed data frames that are to be distributed to several outputs. The different lines may be running various interfaces, e.g. E1, E2, E3 and STM-1 (figure 1). Additionally, the data speed of each input line may vary in a wide range. The transition of data frames in the switches is often executed by means of time slot buses (TDMs) located on the back plane of the switches. A TDM bus has a total capacity in the size typically about 1Gbit/s, where each time slot contains 64kbit of data.

A traditional TDM-bus application consists of a data bus (usually 8 bits), a data clock and a frame synchronisation signal. The time domain is divided into frames where each

frame has a fixed duration (usually 125 µs). A frame synchronisation signal indicates the start of each frame and has a period as long as the frame duration. The frame synchronisation signal and the data clock come from a synchronisation master source and form the timing master signals for all transmitters and receivers that are communicating via the TDM-bus. The frames are divided into a fixed number (n) of time slots (TS) identified by local time-slot counters. The local time-slot counters are reset by the FS signal. In each TS, data may be transmitted from a transmitter to a receiver using time division multiplexing (TDM). Serial data coming from data lines are paralleled (8 bits) so that the data can be mapped into the time slots.

In prior-art implementations of components as described above, there are limitations in the flexibility of synchronous digital switches with respect to minimum delay and configuration flexibility when combined with a non-blocking concept, multi-slot switching, high capacity and high reliability.

The international patent application WO 99/59276 describes a synchronous digital switch with improvements compared with commercial available components using switching matrix schemes with a centralised architecture.

The addressing method given in WO 99/59276 is superficially described. Using only a 2-bit RAM for each timeslot gives a limitation on how timeslots can be cross connected (switched) between two line boards. It is, for instance, not described how to change the order of the time slots.

Summary of the invention

It is an object of the present invention to provide an arrangement that eliminates the drawbacks described above. The features defined in the claims enclosed characterize this method.

Brief description of the drawings

In order to make the invention more readily understandable, the discussion that follows will refer to the accompanying drawings.

Figure 1 is a block diagram illustrating an example of serial output/input lines with variable interfaces connected to a TDM bus, e.g. in a switch,

Figure 2 shows how pointers are allocating the memory space of a TDM buffer according to the present invention,

Figure 3 shows three different TDM buffer blocks with associated connection tables at the receiving side of three TDM buses,

Figure 4 shows an example of an entry in a connection table at the receiving side of the TDM buses according to the present invention,

Figure 5 shows three different TDM buffer blocks and one shared connection table at the transmitting side of three TDM buses,

Figure 6 shows an example of an entry in a connection tables at the transmitting side of the TDM buses according to the present invention.

Detailed description of preferred embodiments

In the following, a preferred embodiment of the present invention will be described. This is just one of many embodiments and variations within the scope of the invention defined by the independent claims enclosed, and must not be considered as limiting.

The preferred embodiment resides in a switch with I/O lines of various interfaces as shown in figure 1. There are three buses in the back plane, and the incoming data shall be distributed among them. There are 8192 time slots per frame available on each bus (66MHz), which makes 24576 time slots all together.

The incoming data will be buffered in one set of memory blocks for each bus. The physical size of the memory blocks is set at 2048 bytes, which means that the system can handle a maximum of 2048 different bytes (time slots) per frame. The memories are configured in advance with a pointer value for every active line as illustrated in figure 2.

The pointer value holds the address where the first byte in a frame is supposed to be stored. This address is loaded into a local pointer at the start of a new frame, and the pointer is incremented after data has been written to this address. The memory can be shared by 32 different lines, but can also be occupied by only one.

Referring to figure 3, in addition to the memory blocks, there is one connection table associated with each, containing 8192 entries. Each entry has one address field and one control field. The address field points to the location in the memory where the data that are to be read from the memory can be found, while the control field holds information about e.g. whether the current timeslot is enabled, whether it is a minimum delay timeslot, etc.

When reading data from the memories, a time-slot counter is used to index the connection tables. The counter is synchronized to the bus clock, and is incremented along with the time-slots in the back plane. The back plane bus can transfer three different bytes at a time (one byte per bus), so the current connection table entry will relate to timeslots x, x+1, and x+2 in parallel.

The order of the bytes with which they are placed on the bus is the same as the order of their associated addresses in the connection table. Thus, the byte sequence of the TDM buses, and hence also the switching of data from input to output lines are controlled by where the addresses are stored in the connection table. This is pre-arranged by software according to the switching requirements concerned.

An entry in the connection table of the receiving side is shown in figure 4. The entry consists of the following fields:

ADDRESS	addressing a byte in a memory block
EN	enable time slot. Set to '1' if the time slot is enabled and the corresponding data shall be put onto the back plane bus.
MIN	Indicates if the timeslot is minimum delay.
CPU	Indicates if data should be fetched from a CPU register

The term "minimum delay" expresses a mode of the switch in which fast data transfer is given high priority. In normal delay mode, data is stored in one frame and put on the bus in the next one. In other words, two memories are required, each containing 2048 bytes. However, in minimum delay mode, only one memory is required, since data shall be put onto the bus as fast as possible. The software programmer has to make sure that within in the same frame, a data location is not read before write-in. Minimum delay should be configured on line level and not on time-slot level.

So far, only the receiving side of the TDM buses has been described. According to the present invention, a similar architecture is present at the transmitting side, as shown in figure 5. The modules shown are responsible for storing

data coming from the back plane bus, and pass it on to the outgoing lines.

As already mentioned, there are three buses in the back plane, and each of them can have 8192 time slots (66 MHz). This makes 24576 time slots all together. The data coming from the back plane will go to one memory block per bus, and a connection table then addresses these memories. As opposed to the receiving side, there is only one connection table, and not one per bus. However, the transmitting side connection table also contains addresses and control bits. The addresses are used to point to locations in the memory blocks, while the control bits can be used to set minimum delay.

The size of the connection table is set at 2048 bytes, which means that the system can handle a maximum of 2048 different bytes per frame. The connection table is configured in advance with a size parameter and a pointer value for every active output line. The pointer value holds the address where the first memory address can be found. This pointer value is loaded into a local pointer at the start of a new frame, and the pointer is incremented after data has been fetched from the location the pointer is addressing. The connection table can be shared by 32 different lines, but can also be occupied by only one. The size parameter controls the connection table allocation.

A timeslot counter is used to index the large memory when fetching data from the back plane bus. Since there are three buses, three data bytes have to be fetched in parallel. The order of the addresses in each part of the connection table then controls the output order of the corresponding bytes in the respective output lines.

Also, at the transmitting side, minimum delay means that only one memory block per TDM bus is used, since data shall be put onto the bus as fast as possible. The software pro-

grammer has to make sure that a data location is not read before write-in within in the same frame.

32 dedicated CPU registers are available for storing idle pattern data. These patterns can be sent out on the serial lines.

An entry in the connection table of the transmitting side is shown in figure 6. The entry consists the following fields:

ADDRESS	the addressing of the RAM
MIN	Indicates if the timeslot is minimum delay
BUS	"00" - fetch data from bus 1 "01" - fetch data from bus 2 "10" - fetch data from bus 3 "11" - fetch data from a CPU register

The present invention provides full flexibility to cross connect time slots, and any combinations of time slots can be transferred between lines (changed order and number of time slots) depending on how the connection tables are configured to write to and read from the TDM bus.

Further, the delay through the node can be very low when using minimum delay. In fact, it can be less than 40µs? for a 2Mbit/s connection. In minimum delay mode, the system is not non-blocking.

The present invention allows for an increase in back plane speed, and high capacity can be implemented at a relatively low cost.

Also, redundant TDM bus, multicasting and broadcasting (one transmitter and several receivers) are permitted.

Abbreviation

E1	2 Mbit/s data transfer method
LINE	Serial data lines, i.e. E1, STM-1 etc.
PFU	Power Feeding Unit
STM-1	Synchronous Transfer Mode
TDM	Time Division Multiplexing